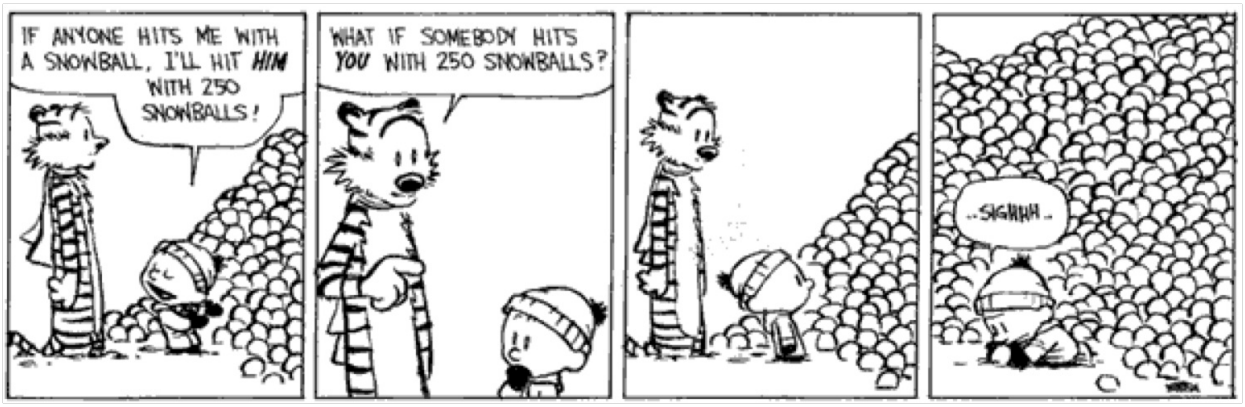
# Meeting 7: Register Allocation




## Announcements

- HW2 due today at 6pm
  - Same submission as HW1
- HW3 due 9/~~22~~ 29 -- start today! -2 week lab

## Submission

- Sign-up for interview
- Code
  - Submit (push) to GitHub
  - Submit zip on COG (as many times as you like)
  - Upload zip to Moodle
- Test
  - Submit (push) tests to https://github.com/csci4555-f17/pyyc-tests-contrib
- Survey: any non-empty answer to the following will receive full credit for this part of the lab.

## FAQ and Reminders

- Are the interview questions supposed to be "ambiguous"? No.
- Interviews are a learning activity. Work with your interviewer to get the feedback that you need.
- Need to be on-time for interviews with laptop ready. Otherwise, you will not be able to interview.
- Zoom locations are for distance students.

- Too many websites? Moodle is your "home base".
- Course assistant hours: review concepts, discuss instructor tests, discuss reference compiler

## Questions

1. Strategy for new lines (HW2) ✓
2. Parse table out put ✓
3. Liveness analysis

HW1 – HW2 – HW 3

HW1 ↑ PD

HW2 ↑ parser for PD

current compilers variables were on the stack

works but slow!

accessing registers – 1 cycle
cache – > tens
memory – > hundreds

register allocation ↑ optimization

semantics – preserve but (hopefully) faster

x86: 8 registers

9 variables

$x = \ldots$ . {x}
$y = x$

} no longer use x

## liveness

- a variable is live at a location (program location) if it may be read at a later location with no intervening assignment

---

## Environment

$x \rightarrow -4(\%ebp)$ HW1

---

Source (IR) Target (x86)

$x \rightarrow \%ecx$
$y \rightarrow -4(\%ebp)$

← Liveness Analysis

↑ How?

# HW 3

## HW 1 | 2

x, y, z, tmp0, tmp1

Flatten → Instruction Selection → x86 IR (with infinite num / variables)

Flat AST

x86 IR → Register Allocation → x86 IR → print → x86

x86 w/o variables

x and z are not live at same time (or hold the same value)

- x → %eax
- y → -4(%ebp) ← spill
- z → %eax

x and z interfere if they are live at the same time

## register allocation

x86 IR → liveness analysis → map: locations → set of live vars at that location → build an interference graph → color graph → env (registers, allocations)


- eax
- ebp

%eax caller-save register

%edi callee-save register [?]

6 normal use registers

(2 %esp, %ebp)